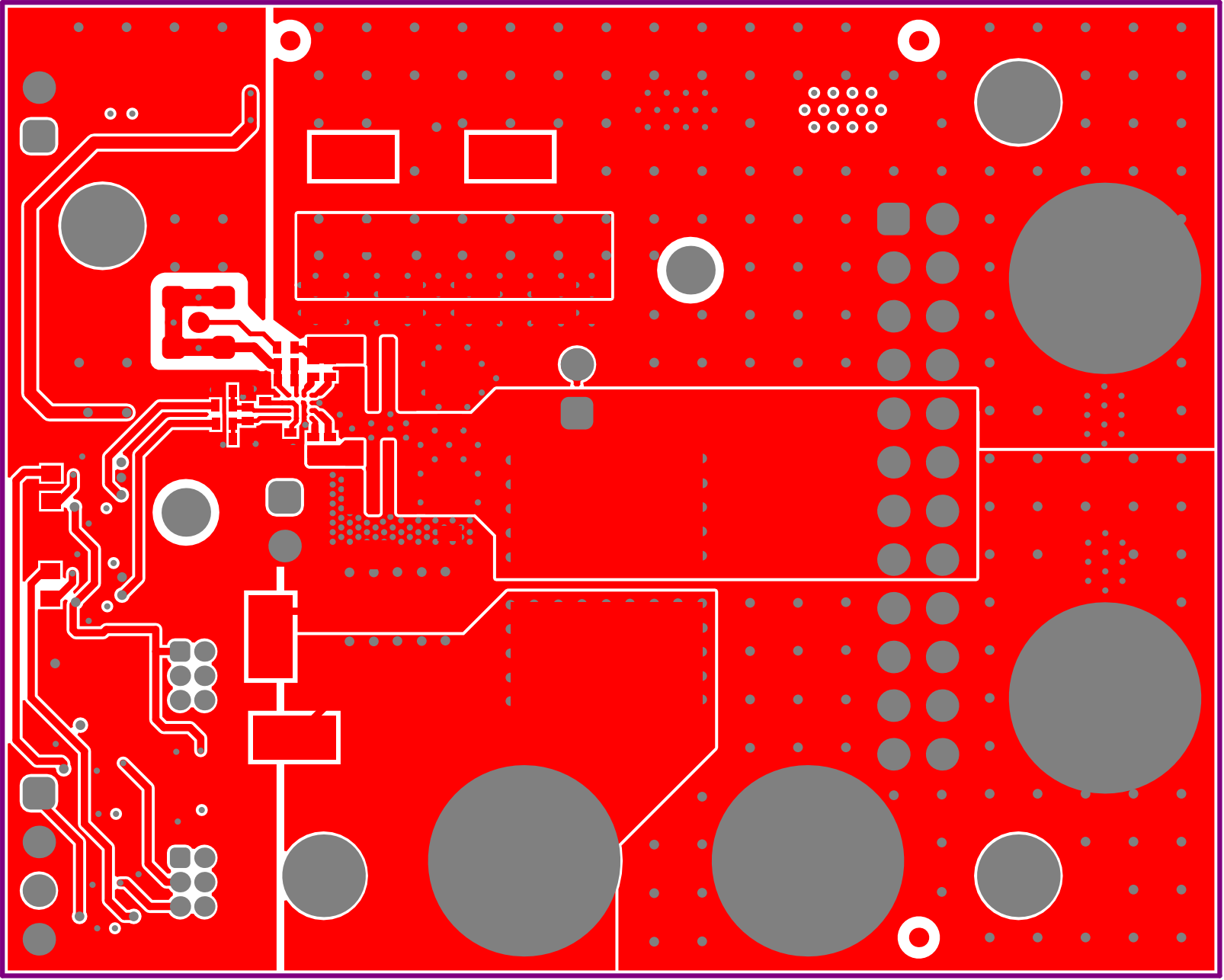
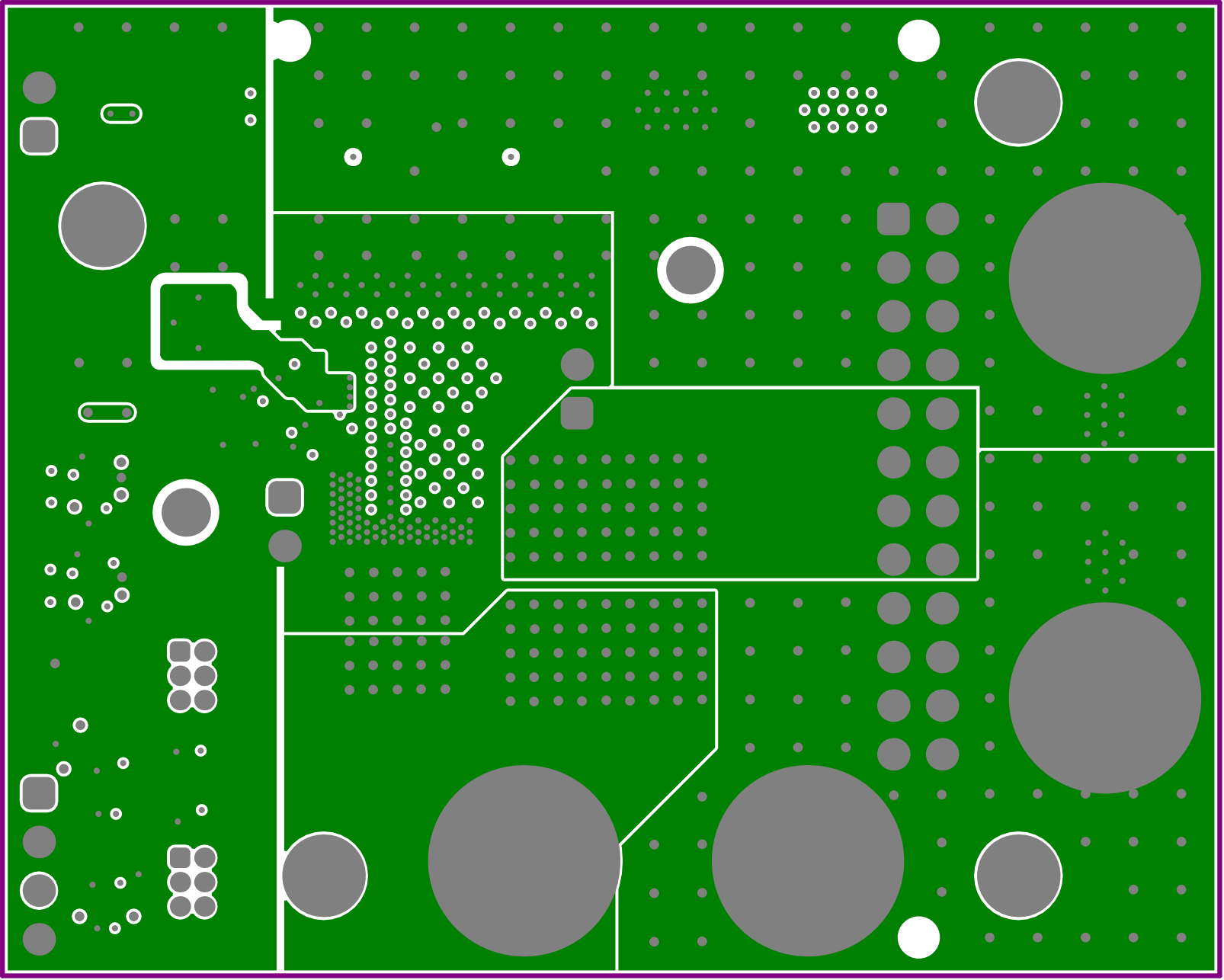
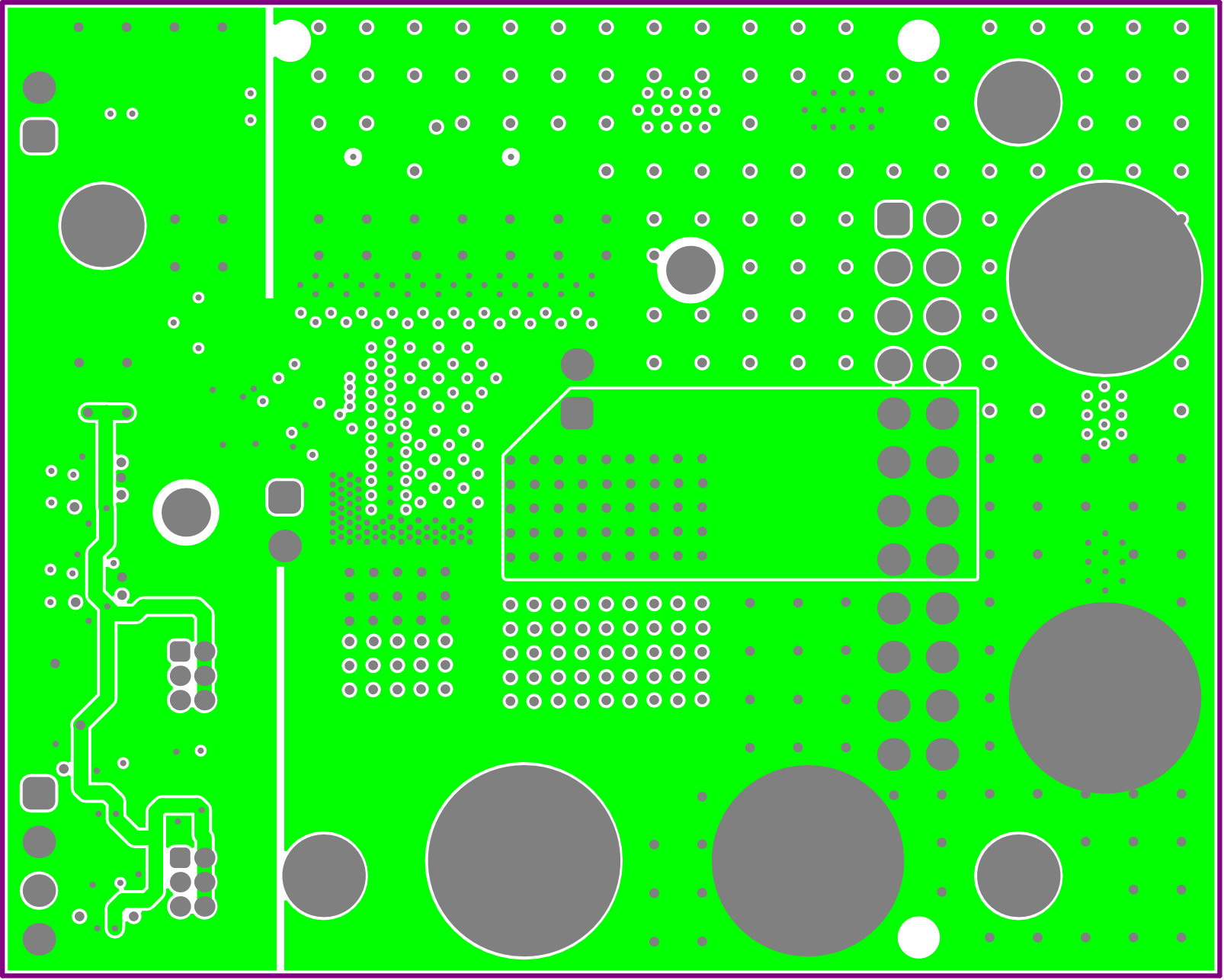
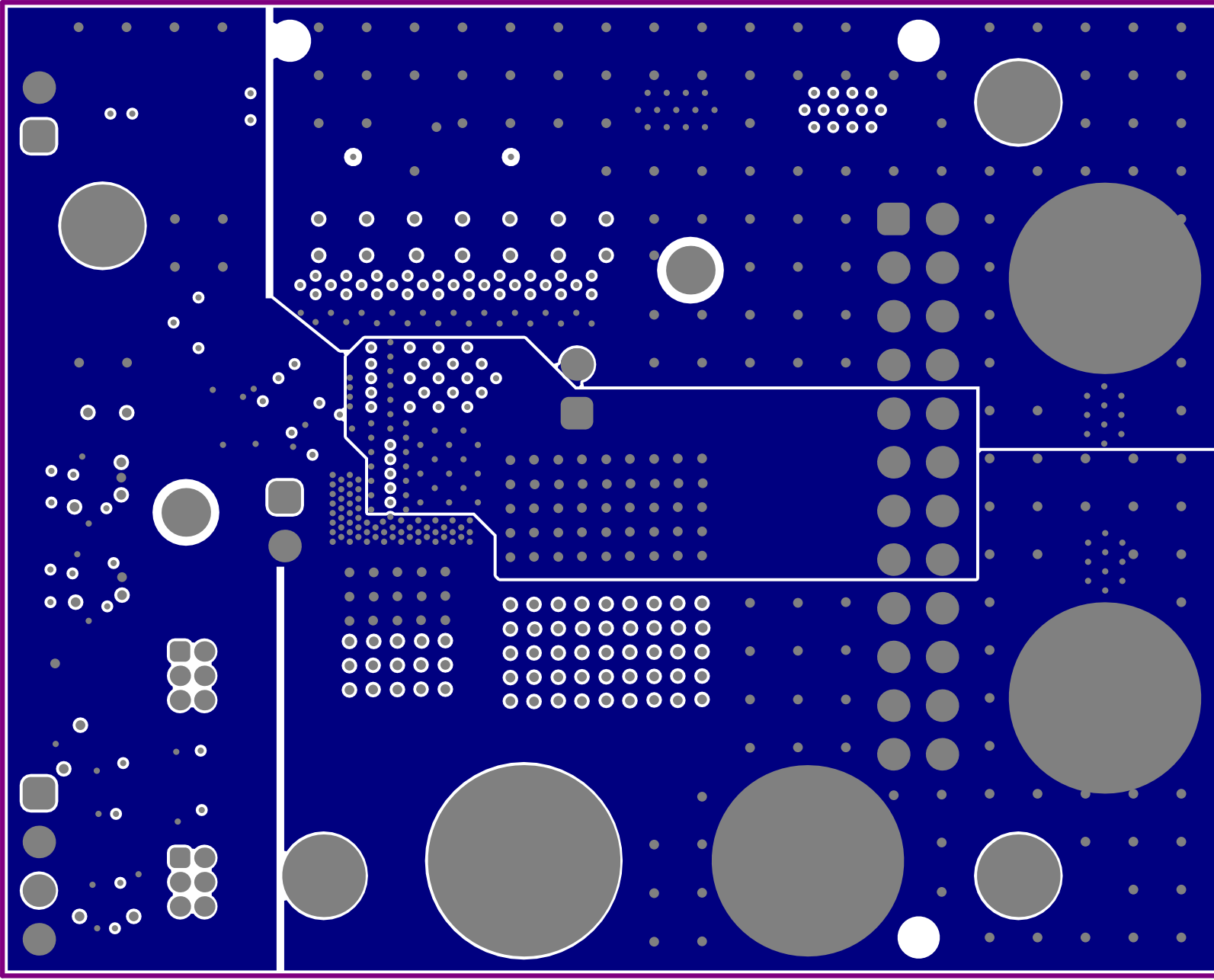
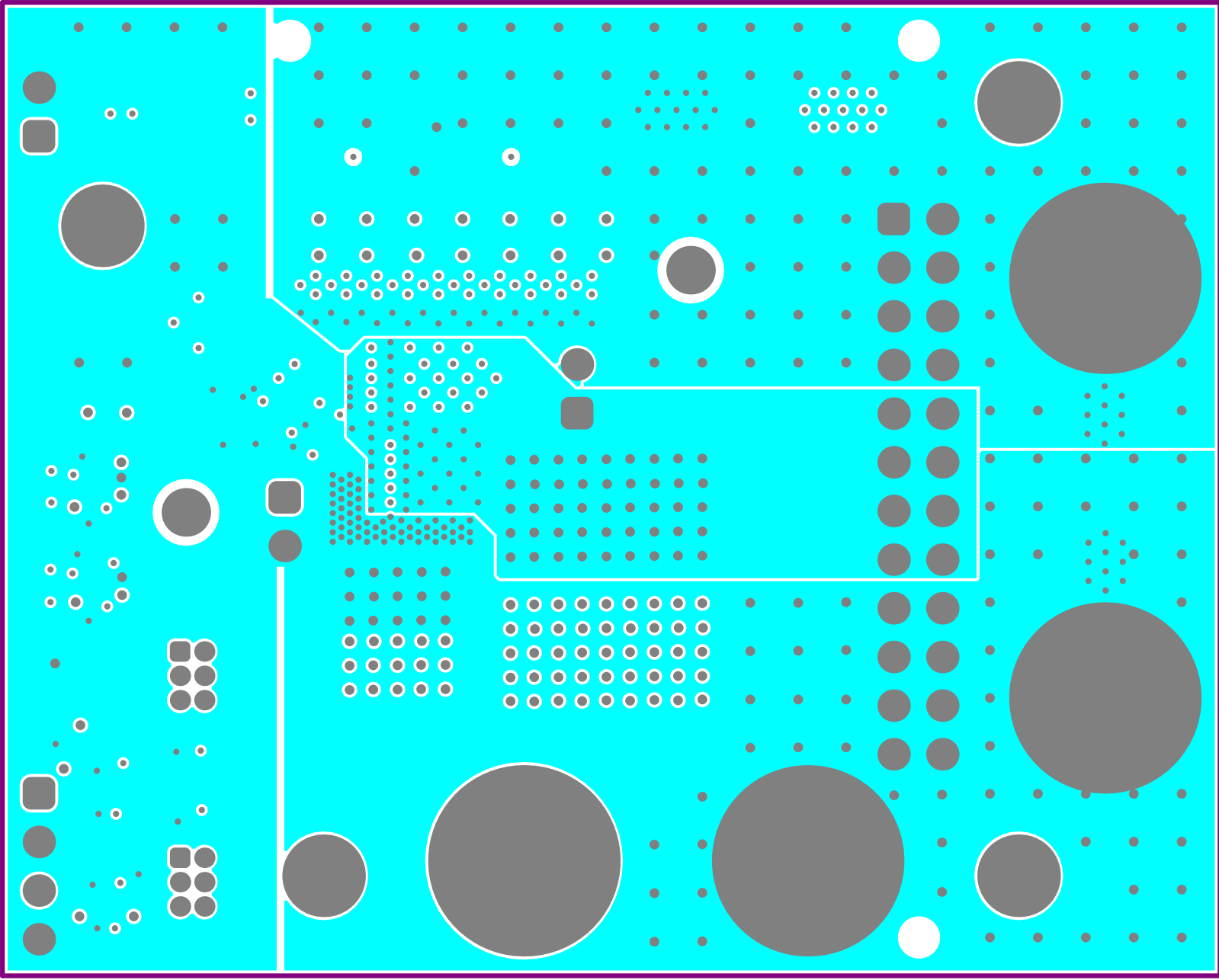


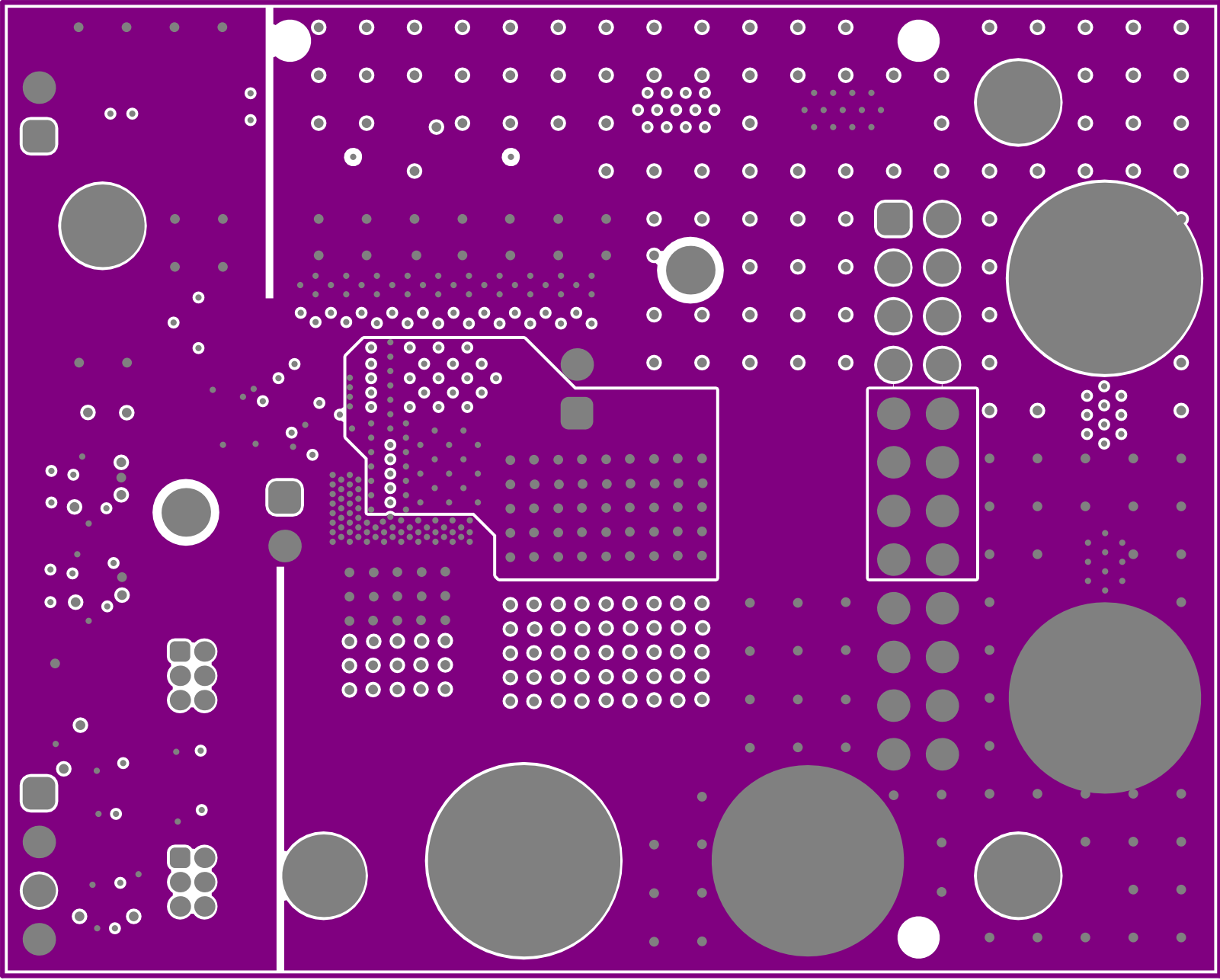


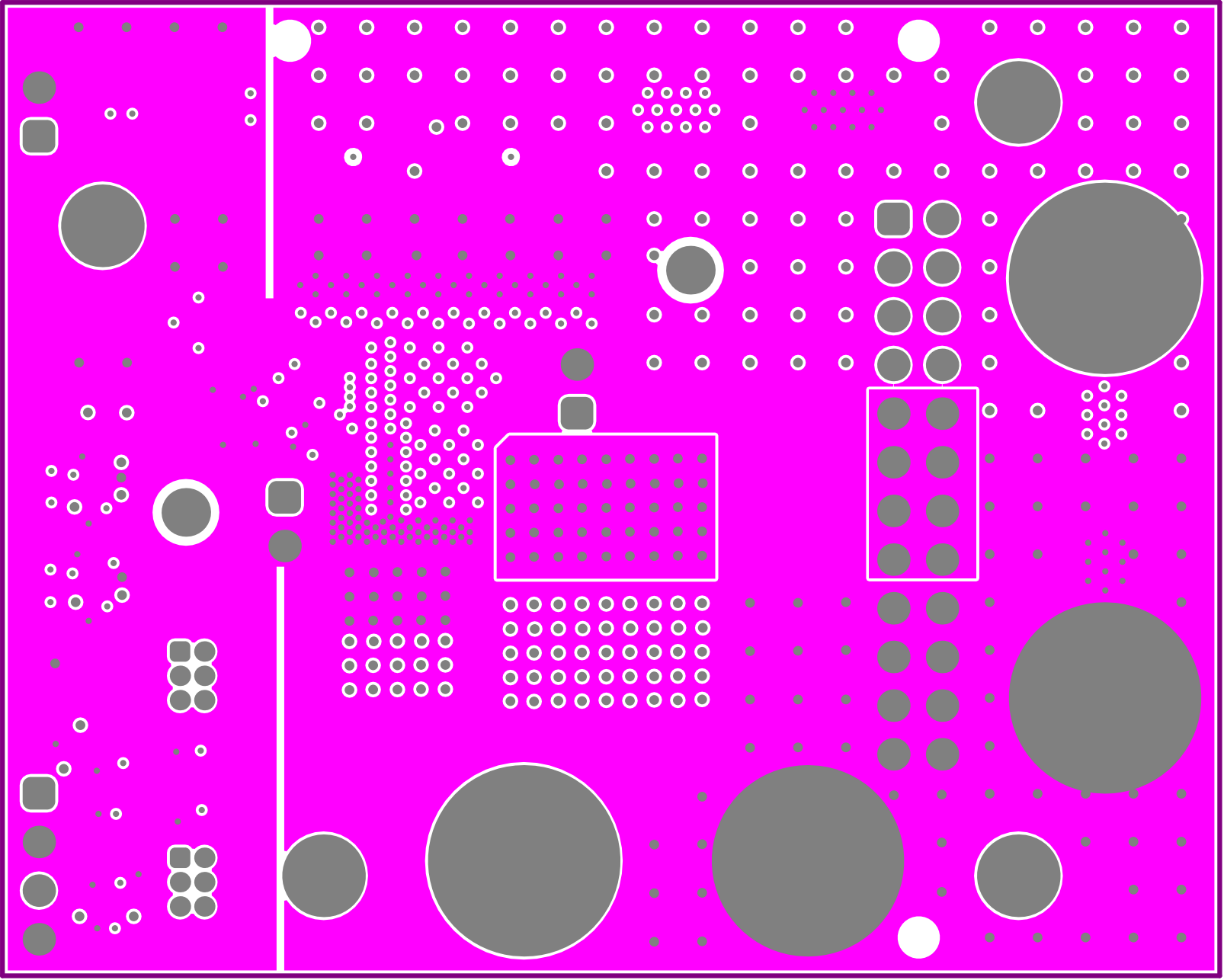


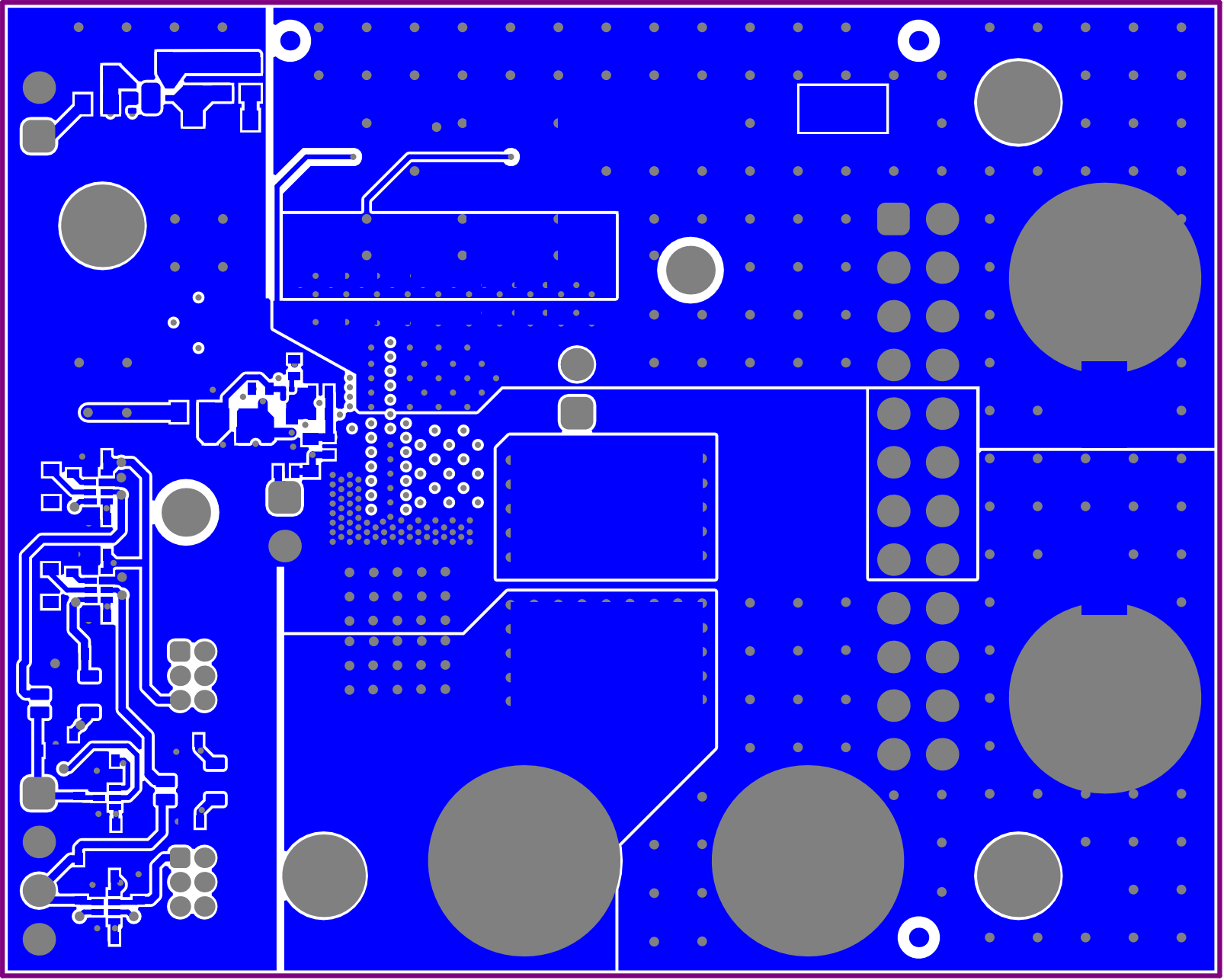












7.5 V - 12V

GND
VDD



EPC90

Rev. 1.0

VIN

GND

TP2
TP1

eGaN® FET

EPC

EFFICIENT POWER CONVERSION

Pbf

S01

V
max.
J6

VIN

VIN

SW

High voltage

GND

J7

L1

GND

GND

S02

J5

© EPC

HS1

VGu

C11 C12 C13 C14 S05 C15 C16 C17 C18 C19 C110 C111 C112

D1

SW
+

Q1

Q2

UG1

J22

S06

D2

GND

Cout

Vout

VOUT

TP3

TP4

J630

S04 J4

Hot Surface

S03

R11 J1

D60

C81

C80

U80

R83R80

R82R81

C75C70

C1

DTupper

R620

R625

DTlower

J640

Full

DT

None

Bypass

PWM1

GND

PWM2

GND

Mode

Buck

Boost

Dual

Mode

J630



ATTENTION
ELECTROSTATIC
SENSITIVE DEVICE

END

13

2m1e

2.1mC

TUOV DNE

$$\frac{133}{W2} +$$

Column

LS

PMO
END
PMO
END

15
R616 C616
R616 U616
R643 R616 C616
R603 R610
1023

Approved for
only; not FCC
For evaluation

BRZ
D93
E2A
C67
B67
D01
R27
C60

879

CWT CWS

|||

41m3
31m3
151m3
11m3

2019 - 2021

DeSO
Ceso

CRJ
URJ
RJR

4025
C911
N911
R902

180
180
180

[illegible]

1469
6841
7812
2812



RESEARCH

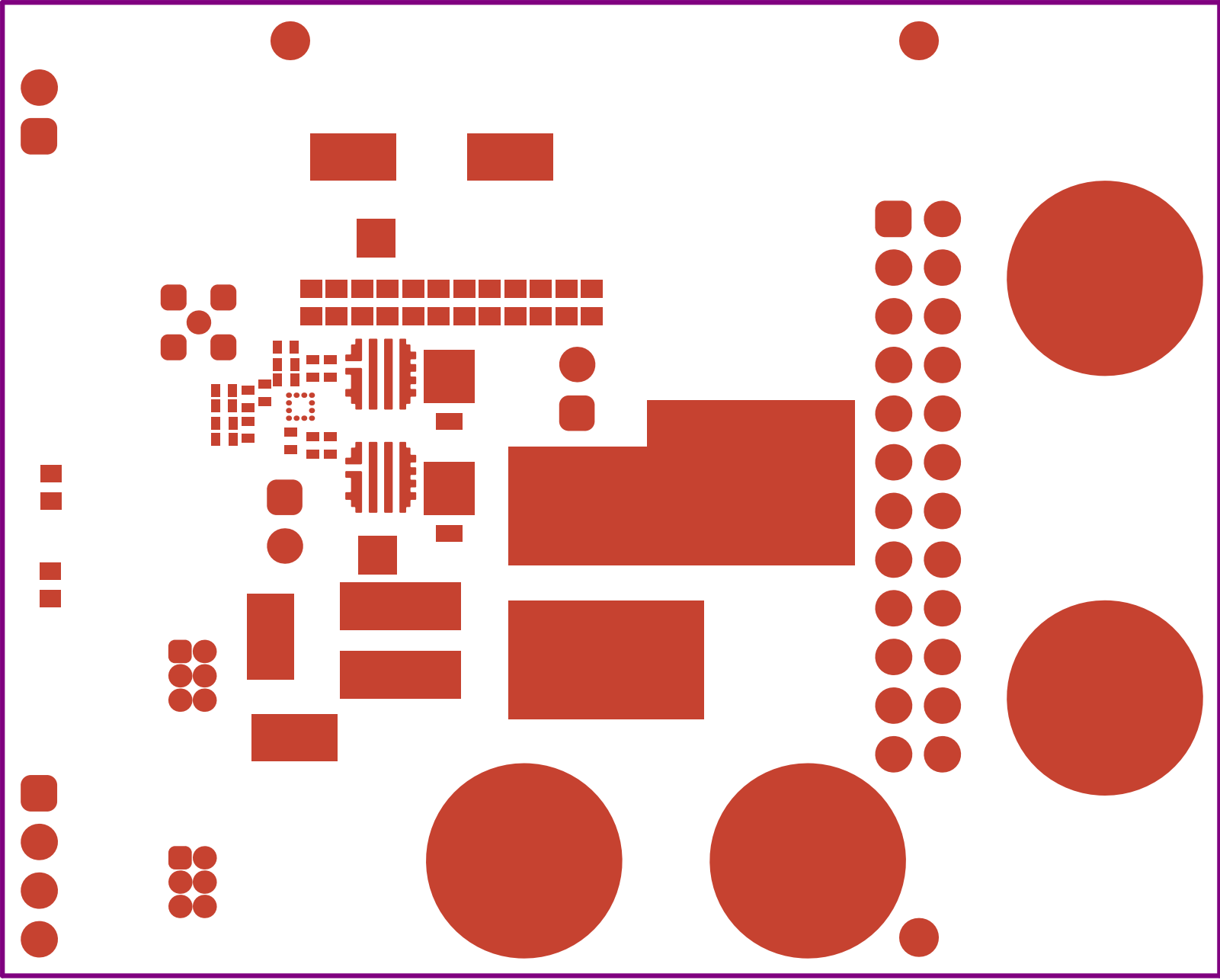
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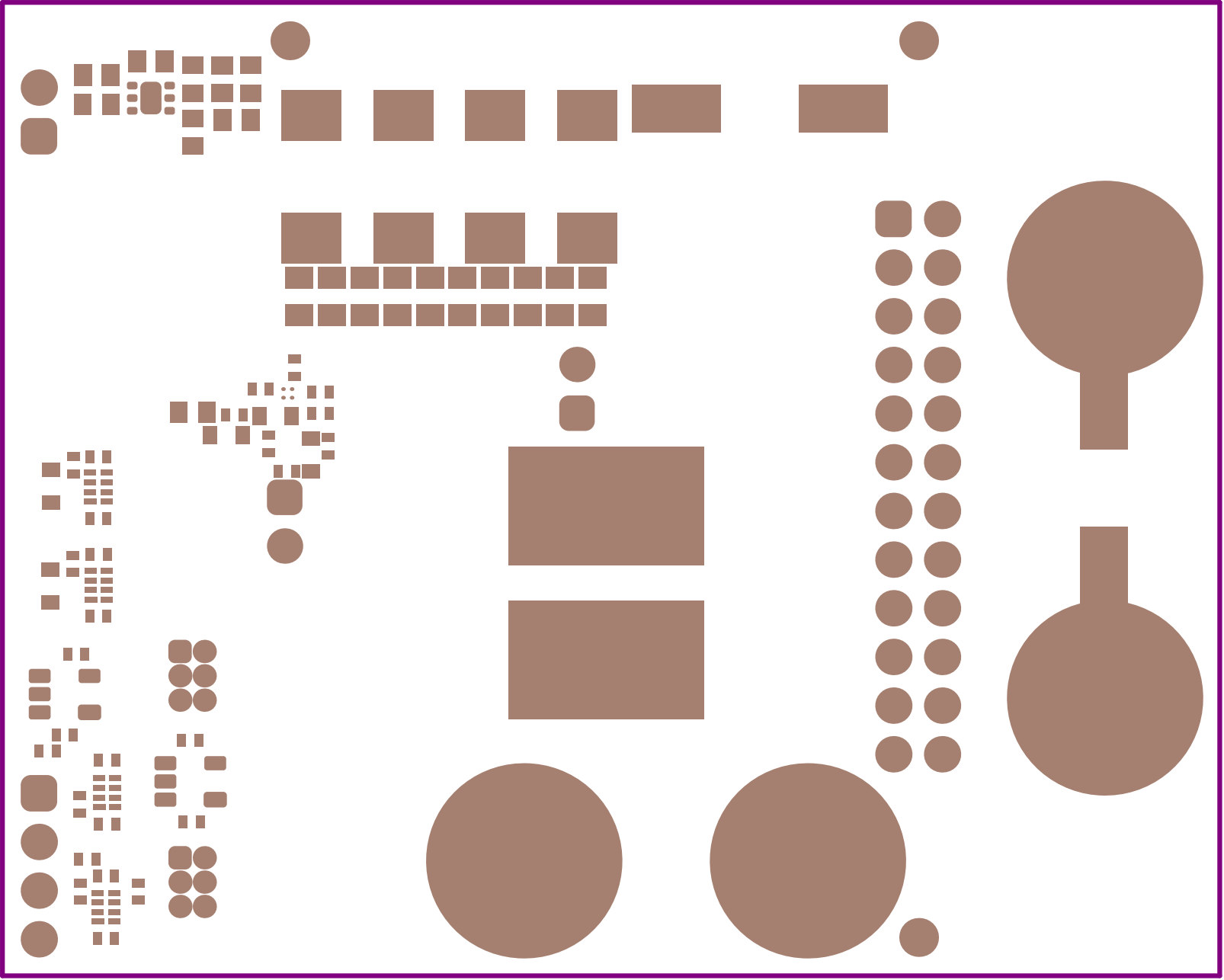


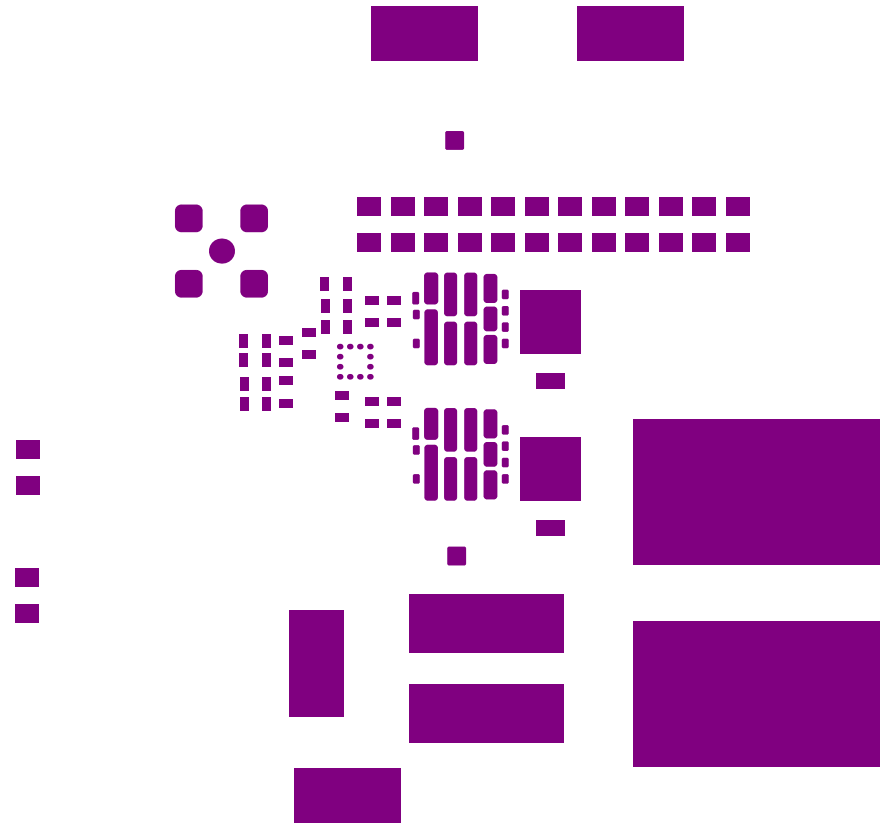
RIO

PCB#: B2523 Rev. 1.0









System Architecture Diagram

The diagram illustrates a system architecture with the following components and connections:

- Central Processing Unit (CPU):** A central block with a clock icon, connected to various components.
- Memory:** A block labeled "Memory" connected to the CPU.
- Storage:** A block labeled "Storage" connected to the CPU.
- Network Interface:** A block labeled "Network Interface" connected to the CPU.
- System:** A large rectangular block on the right side, labeled "System".
- Input/Output (I/O):** A block labeled "I/O" connected to the CPU.
- Peripheral Devices:** Several smaller blocks representing peripheral devices, including a "Printer", "Scanner", and "Mouse".
- Connections:** Solid lines represent direct connections, while dashed lines represent indirect or logical connections.

